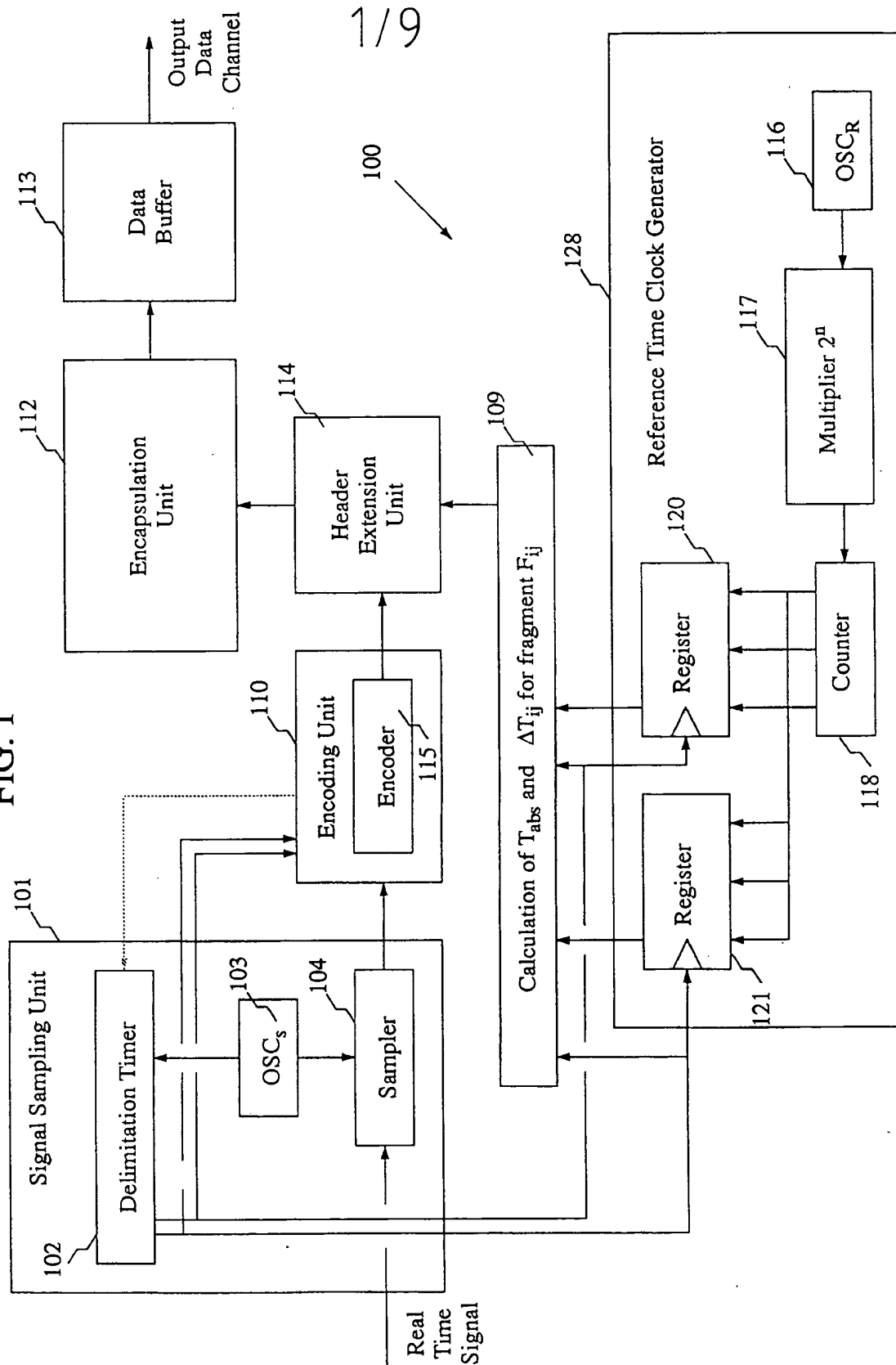
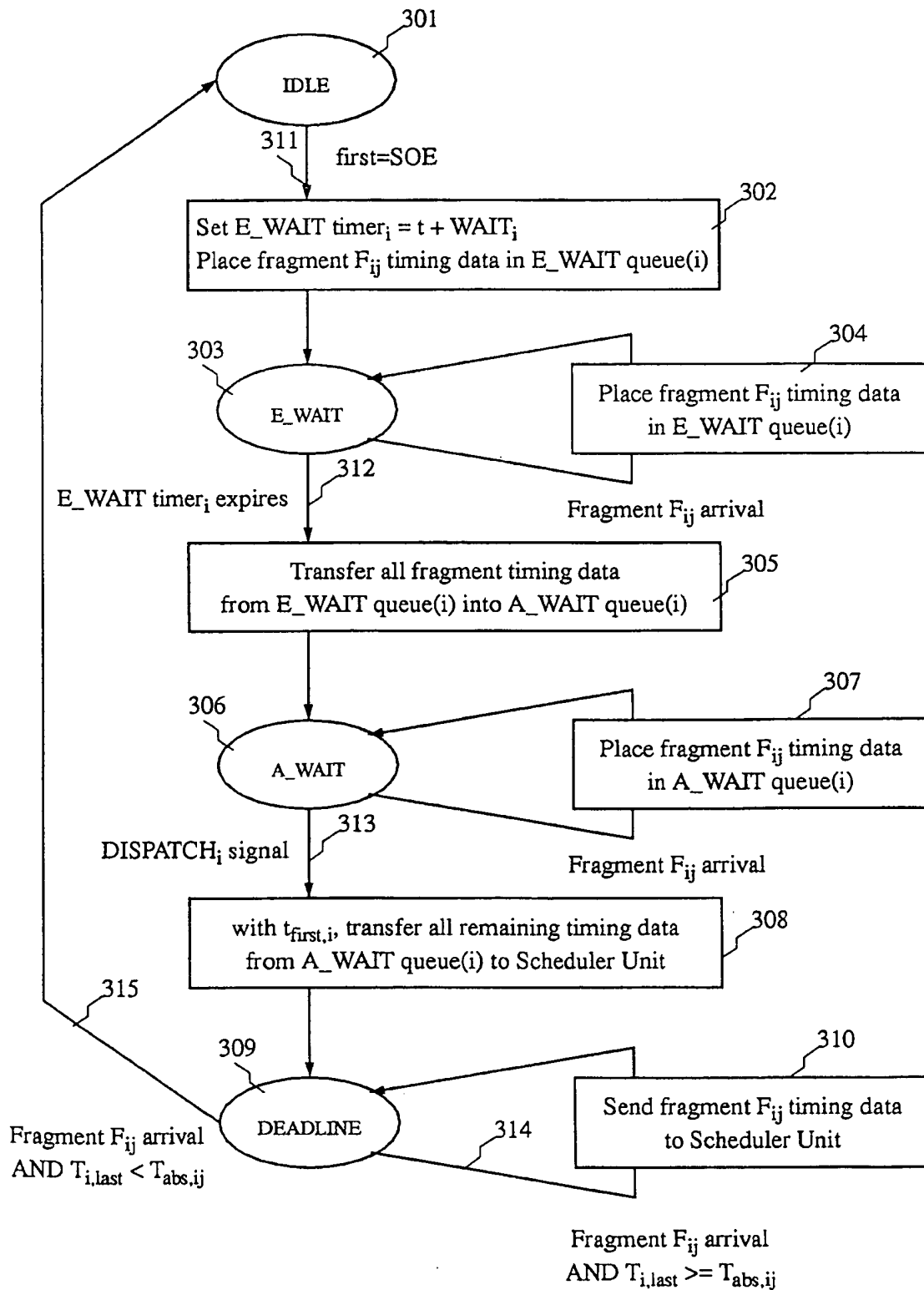
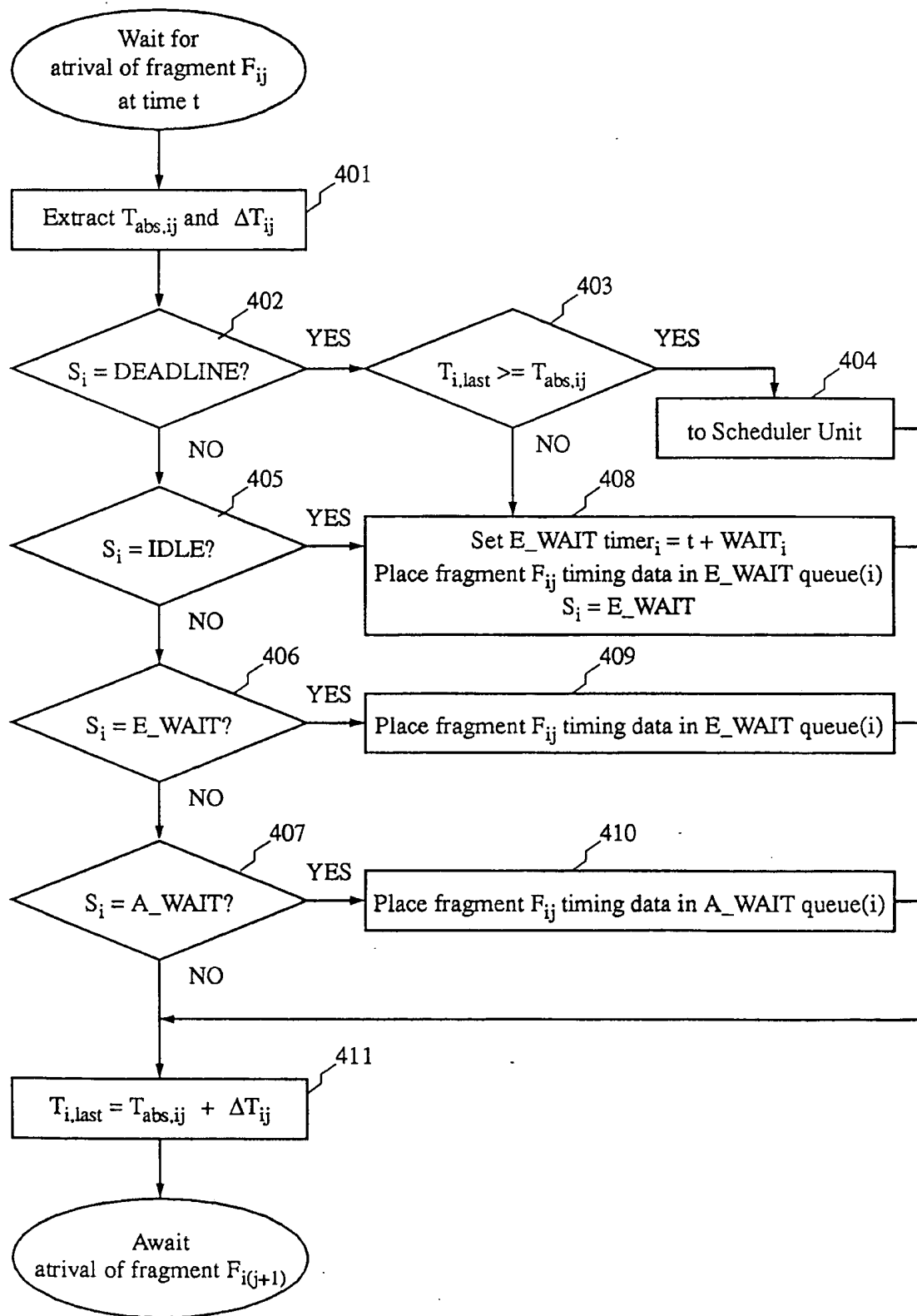


FIG. 1

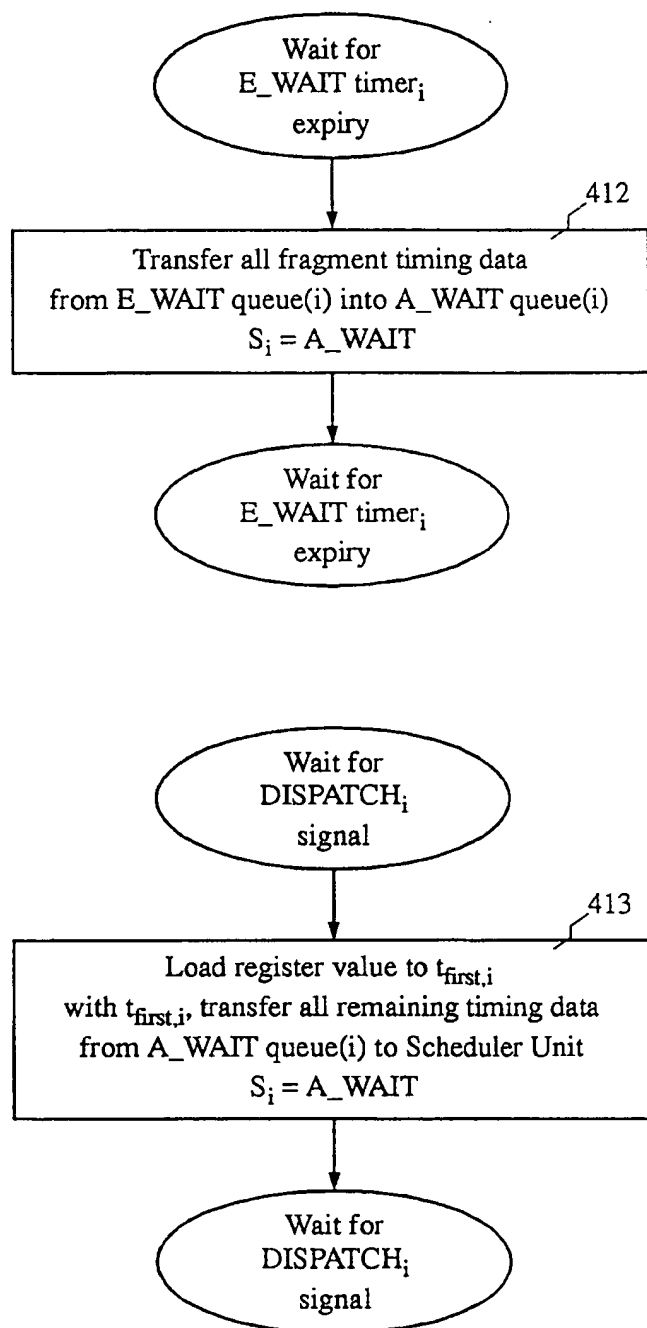


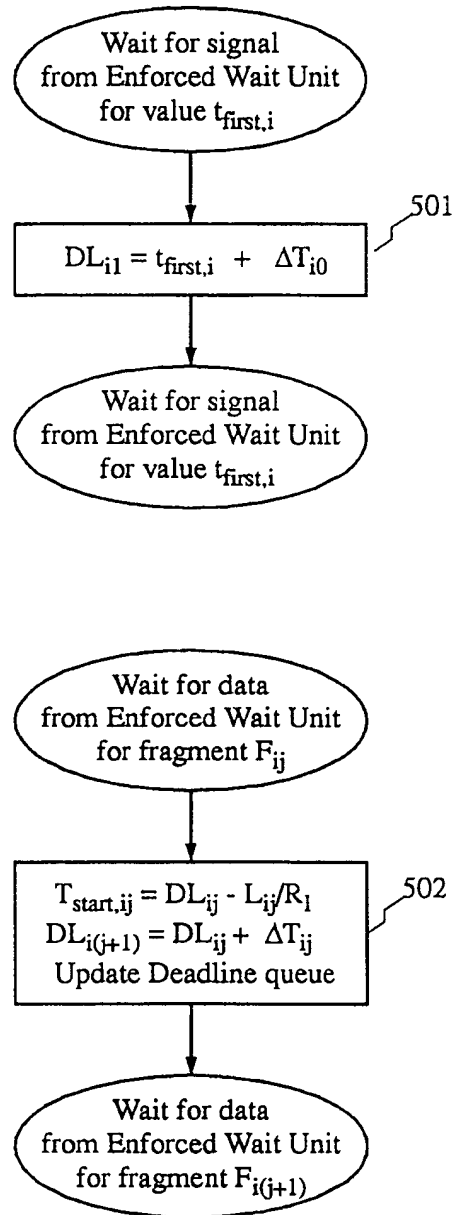
The diagram illustrates a packet scheduling system 200. At the top is the Channel Identification Unit 201. Below it are the Data Control Unit 227, the Scheduler Unit 210, and the Enforced Wait Unit 204. The Enforced Wait Unit 204 contains an E_WAIT Timer 205. To the right of the Scheduler Unit 210 is the Dispatching Unit 228. A Memory Block 211 is located in the center, containing a Fragment Block, a Data Queue 212, a Deadline Queue 213, and a set of queues 214, which includes an A_WAIT Queue(i) and an E_WAIT Queue(i). At the bottom is the Reference Time Clock Generator 206, which includes an OSCr 207, a Multiplier 2ⁿ 231, a Register 224, and a Counter 208. Signal lines connect the various components: from the Channel Identification Unit 201 to the Data Control Unit 227, Scheduler Unit 210, and Enforced Wait Unit 204; from the Data Control Unit 227 to the Fragment Block and Data Queue 212; from the Scheduler Unit 210 to the Deadline Queue 213 and the queues 214; from the Enforced Wait Unit 204 to the E_WAIT Queue(i) and the Reference Time Clock Generator 206; from the Reference Time Clock Generator 206 to the Enforced Wait Unit 204 and the Dispatching Unit 228; and from the Dispatching Unit 228 to the Fragment Block and the queues 214.

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FIG. 3

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FIG. 4(a)

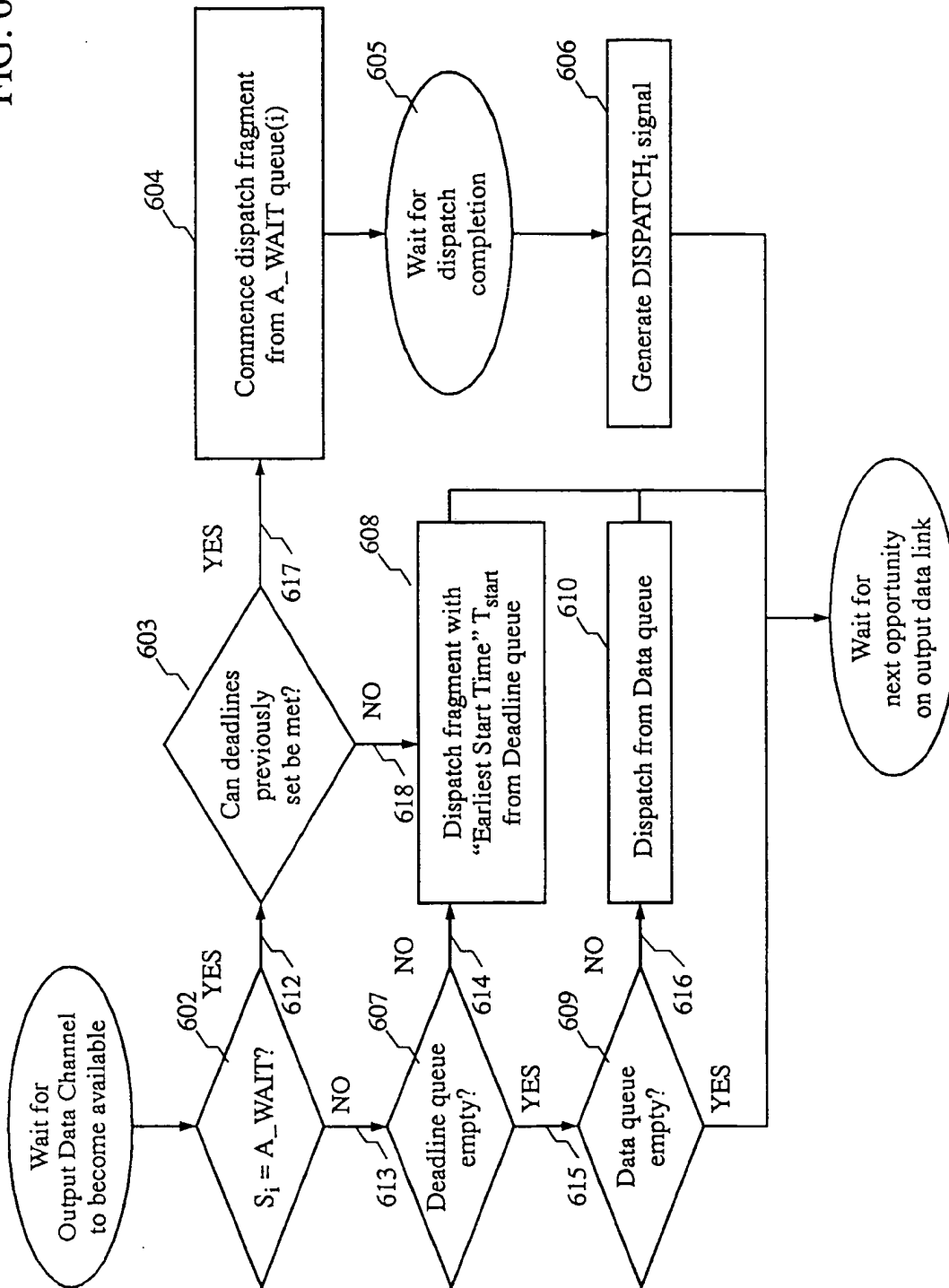
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FIG. 4(b)



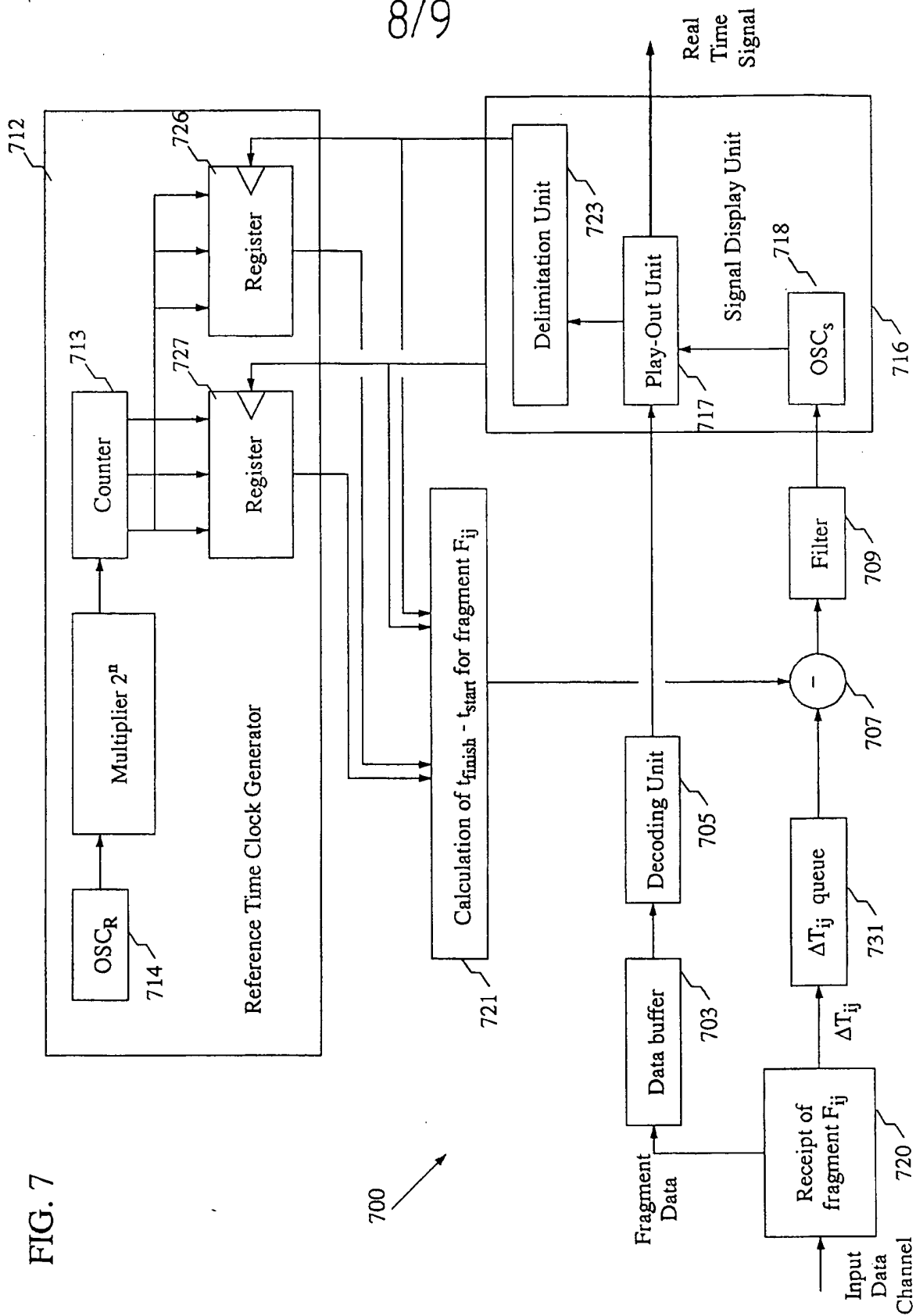
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FIG. 5

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FIG. 6



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FIG. 8

